REMARKS

Claims 1, 5-9, 11, 14-18 and 21-27 are pending in the present application. By this reply, claims 2-4, 10, 12-13 and 19-20 have been cancelled and new claims 21-27 have been added. Claims 1, 11 and 18 are independent claims.

The specification and claims have been revised to correct minor informalities and to clarify the invention. These modifications do not add any new matter to the disclosure.

DRAWINGS

As required by the Office Action, corrected formal drawings are submitted herewith in a Letter to the Official Draftsperson in response to the Examiner's approval of the drawing corrections filed on January 28, 2002.

35 U.S.C. § 112, SECOND PARAGRAPH, REJECTION

Claims 3, 4, 8, 11-13, 16, 19 and 20 have been rejected under 35 U.S.C § 112, second paragraph, as being indefinite. This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

Regarding the features "connected to Vcc" and "connected to Vss", Applicants respectfully submit that such features do not render the claims indefinite because the terms Vcc and Vss are widely used and known terms in the art. Further, the original specification clearly discloses in one embodiment what Vss and Vcc represent. For example, page 2, line 20 of the specification teaches "a ground Vss"

and page 11, line 8 teaches "Vcc reference voltage" (i.e., non-ground voltage). Nevertheless, the claims have been amended to clarify the invention with respect to the use of these terms only to expedite prosecution.

Regarding the Examiner's objection to the use of the term "substantially", Applicants respectfully submit that the use of the term "substantially" does not render the claims indefinite because one of ordinary skilled in the art would know what was meant by "substantially parallel" and "substantially same shape". See MPEP 2173.05(B) which permits the use of the term "substantially" in the claims.

Based on these reasons, reconsideration and withdrawal of the rejection is respectfully requested.

35 U.S.C. § 102 REJECTION

Claims 1-3, 5-12 and 14-19 have been rejected under 35 U.S.C § 102(e) as being anticipated by *Tsukude* (U.S. Patent No. 6,191,461). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

The Examiner alleges that *Tsukude* teaches a second active region connected to "the power supply node, which is considered to be Vcc" on page 4, line 12 of the Office Action. However, *Tsukude* clearly discloses that the impurity regions 16e, 16f are connected to the power supply node which is a ground node (Vss) (column 9, lines 48-49 and lines 63-66). It is well established in the art that Vcc represents a non-ground voltage. Furthermore, the Examiner states that the

impurity regions 16e, 16f "must inherently be n-type in order to establish a field transistor between the two regions" on page 4, lines 15-16 of the Office Action.

Therefore, *Tsukude* fails to teach or suggest, *inter alia:*

> the second active region includes an n+ junction connected to Vcc reference voltage or a p+ junction connected to ground Vss

as recited in independent claim 1; and

> the predetermined conductive type second active region is an n+ junction connected to Vcc reference voltage

as recited in independent claims 11 and 18.

Accordingly, the invention as recited in independent claims 1, 11 and 18 and their dependent claims (due to their dependency) is patentable over *Tsukude,* and reconsideration and withdrawal of the rejection based on these reasons is respectfully requested.

35 U.S.C. § 103(a) REJECTION

Claims 4, 13 and 20 have been rejected under 35 U.S.C § 103(a) as being unpatentable over *Tsukude* in view of *Lee et al.* (U.S. Patent No. 6,097,066). This rejection, insofar as it may pertain to the presently pending claims, is respectfully traversed.

The Examiner acknowledges that *Tsukude* does not teach a second active region including a p+ junction connected to Vss. Therefore, the Examiner relies on *Lee et al. Lee et al.* is directed to a structure shown in Figs. 5 and 6 including four ring-shaped active regions (530, 500 and 510), another active region 550

around these four ring-shaped active regions, and another region 560 around the region 550. The Examiner equates *Lee et al.'s* p+ conductive type active region 550 to Applicants' second active region. The Examiner asserts that it would have been obvious to modify *Tsukude's* device by forming the second active region with a p+ junction connected to Vss in view of *Lee et al.'s* teaching because it provides "a discharge path for an ESD pulse applied to the first active region".

However, *Lee et al.* discloses that the ring-shaped structure 560 (which the Examiner equates to Applicants' third active region) has the same n conductivity as the first active regions (530, 500 and 510). In contrast, in Applicants' claimed invention, the third active region has conductivity type that is different from the conductivity type of the first active region.

Therefore, even if the references are combinable, assuming *arguendo*, the combination of references as applied by the Examiner would still fail to teach or suggest, *inter alia:*

> a third active region surrounding the first and second active regions and being of conductivity type different from that of the first active regions

as recited in independent claim 1 and 18; and

> a predetermined conductive type second active region is an n+ junction connected to Vcc reference voltage

as recited in independent claim 11.

Accordingly, the invention as recited in independent claims 1, 11 and 18 and their dependent claims (due to their dependency) is patentable over the

combination of references as applied by the Examiner, and reconsideration and withdrawal of the rejection based on these reasons is respectfully requested.

CONCLUSION

For the foregoing reasons and in view of the above clarifying amendments, Applicants respectfully request the Examiner to reconsider and withdraw all of the objections and rejections of record, and earnestly solicit an early issuance of a Notice of Allowance.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Esther H. Chong (Registration No. 40,953) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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JAK/EHC:lmh
Enclosure: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The specification has been amended as follows:

Paragraph **[27]** has been amended as follows:

[27] For each active region 200, the drain regions 202 and 205 are connected to an input or output pad, the source region 206 is connected to a ground Vss, and the pair of the gates 203 and 204 are connected to the ground Vss or an output of a pull-down inverter when used as a pull-down transistor. The n+ active region 201 between two active regions 200 is connected to Vcc reference voltage (or ground Vss when the active region 201 is of p+ type).

Paragraph **[38]** has been amended as follows:

[38] Furthermore, the present invention provides n+ (or p+) junctions, which are connected to Vcc reference voltage (or ground Vss), additionally between respective active regions each of which includes a limited number of gates (e.g., two gates). Accordingly, the present invention effectively discharges a positive ESD pulse by a parasitic npn bipolar operation occurring between the n+ junctions of the drain region connected to the pad and the additionally-formed active region.

In the Claims

Claims 2-4, 10, 12-13 and 19-20 have been cancelled.

The claims have been amended as follows:

1. (Amended) A multi-finger type ESD protection device comprising:

a semiconductor substrate;

a plurality of first active regions formed [separately] on the semiconductor substrate; [and]

a plurality [pair] of gates formed in each of the first active regions;

at least one second active region of a predetermined conductive type formed additionally between the first active regions, wherein the second active region includes an n+ junction connected to Vcc reference voltage or a p+ junction connected to ground Vss; and

a third active region surrounding the first and second active regions and being of conductivity type different from that of the first active regions.

5. (Amended) The device of claim 1 [2], further comprising:

a plurality of drain regions formed in each of the first active regions.

8. (Amended) The device of claim 1 [2], wherein the first and second active regions and the gates extend substantially parallel to each other.

11. (Amended) A multi-finger type ESD protection device comprising:

a semiconductor substrate;

a plurality of first active regions formed separately on the semiconductor substrate;

a plurality of gates formed in each of the first active regions; and

at least one predetermined conductive type second active region [each] formed between two of the first active regions, wherein the predetermined conductive type second active region is an n+ junction connected to Vcc reference voltage.

17. (Amended) The device of claim 11, further comprising:

a third active region surrounding completely the first and second active regions.

18. (Amended) A multi-finger type ESD protection device comprising:

a semiconductor substrate;

a plurality of first active regions formed separately on the semiconductor substrate;

a plurality of gates formed in each of the first active regions;

[drain regions formed at n+ junctions of both end portions of the first active regions;

source regions each formed between the pair of gates in each of the first active regions; and]

at least one second active region of a predetermined conductive type, formed between the first active regions, wherein the predetermined conductive type second active region includes a p+ junction connected to ground Vss; and

a third active region surrounding the first and second active regions and being of conductivity type different from that of the first active regions.

Claims 21-27 have been added.